



Intel® 31154 133 MHz PCI Bridge Documentation & SROM Issue

May 6, 2005

The purpose of this document is to provide information on a recently discovered 31154 Bridge documentation discrepancy and also an error in the default serial ROM code and help files provided as part of the 31154 Bridge software tools distribution. This problem will be listed in the next revision of the 31154 specification update, as a documentation clarification and updated in a new evaluation board software tools distribution.

Intel® 31154 133 MHz PCI Bridge Masquerade Feature Application Note and SROM code is incorrect

- Problem:** The Intel® *31154 133MHz PCI Bridge Masquerade Feature Application Note*, Page 7, Section 6 first Note, indicates that “Reserved or unused bits must be written to 0b when formatting the Serial ROM contents”. This is incorrect.
- The statement should read “Reserved or unused bits must be written per the values defined in the *Intel® 31154 133MHz PCI Bridge Developer’s Manual*.” The Intel-provided reference code will set the reserved bit of VCR1at offset 44h bit 5 to 0b. This bit must be set to 1b for proper operation of the bridge.
- The help file associated with the SROM programming tool also incorrectly specifies the value of the register.
- Implication:** The bridge may not operate properly under all conditions.
- Workaround:** If using the DefaultData.dat image provided as part of the evaluation card software and tools zip file, make sure that VCR1at offset 44h bit 5 is set to 1b. The latest revision of the software on the Intel website has been updated with a corrected value for this register. Please download the current version of the evaluation card software and tools zip file from the website to get the latest, corrected release.
- Status:** The documentation, SROM image (DefaultData.dat) and the help files will be updated to correct this issue.

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